REMARKS/ARGUMENTS

Claims 1, 2, 4, 6-14, 16-18, 20-22 are pending. Claims 1, 8, 9, 13, 18, 21, and 22 have been amended.

1. Summary of the Office Action

Claims 18 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-2, 4, 6-11, 13-14, 16, 18, 20-22 stand rejected under § 103(a) as being unpatentable over U.S. Patent No. 5,954,815 (hereinafter "Joshi") in view of U.S. Patent No. 4,682,284 (hereinafter "Schrofer").

Claim 12 is rejected under § 103(a) as being unpatentable over Joshi in view of Schrofer and further in view of U.S. Patent No. 6,477,562 (hereinafter "Nemirovsky").

2. Response to § 112 Rejections

Claims 18 and 22 have been amended to address rejections under 35 U.S.C. 112. It is respectfully requested that the rejections be withdrawn.

3. Response to § 103 Rejections

Claim 1, as amended, recites "the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions." The Office action mailed November 24, 2004 correctly stated that Schrofer fails to disclose the first instruction of the plurality of instructions being

indicated as invalid on account of being outside a trace of instructions. Similarly, Schrofer fails to disclose "the first microinstruction ... being indicated as invalid on account of being outside a trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace," as recited in the amended claim 1. The Office action combined Schrofer with Joshi in order to show the features of claim 1.

Joshi discloses a branch instruction comprising two instructions. The first instruction, termed the initial branch instruction, computes the branch target and the branch condition. The second instruction, termed a delay instruction, immediately follows the initial branch instruction and is used to actually change the program flow to the branch target instruction. (Joshi, 6: 45-51.) In Joshi, if the branch is predicted, all instructions in the current line that occur after the delay instruction associated with the branch are invalidated. (Joshi, 7: 2-8.)

However, neither the initial branch instruction, nor the delay instruction associated with the initial branch instruction in Joshi comprises a linear address to determine a set of subsequent entries in the trace. Therefore, neither the initial branch instruction, nor the delay instruction is a head entry within a trace. Thus, the combination of the initial branch instruction and the delay instruction in Joshi is distinct from a trace of microinstructions recited in claim 1. Consequently, Joshi, whether considered separately or in combination with Schrofer, fails to disclose or suggest "the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace," as recited in claim 1, as amended.

Because not every element is disclosed in the combination of Schrofer and Joshi, claim 1 and its dependent claims are patentable over the combination of Schrofer and Joshi and should be allowed.

Claims 13 and 21 recite "a trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace." Thus, claims 13 and 21, as well as their respective dependent claims, are patentable over the combination of Schrofer and Joshi for at least the reasons articulated with respect to claim 1.

Claim 12 stand rejected under §103(a) as being obvious over Joshi in view of Schrofer and further in view of Nemirovsky. Nemirovsky is directed at a multi-streaming processor having resources adapted to execute multiple instruction streams in parallel from multiple available program threads. Nemirovsky fails to disclose or suggest "the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace" present in claim 12 by virtue of its being dependent on claim 1. Thus, claim 12 is patentable over Joshi, Schrofer, and Nemirivsky combination, for at least the reasons articulated with respect to claim 1.

In light of the above, Applicants respectfully submit that the rejections under 35 U.S.C. §103 have been overcome, and withdrawal of these rejections is therefore respectfully requested.

4. Conclusion

Having tendered the above remarks, Applicants respectfully submit that all rejections have been addressed and that the claims are now in a condition for allowance, which is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact Elena B. Dreszer at (408) 720-8300.

Respectfully submitted,

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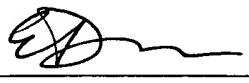

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